Reg.No. \_\_\_\_\_\_\_\_\_\_\_\_



**UNIVERSITY**

(Karunya Institute of Technology & Sciences)

(Declared as Deemed-to-be University under Sec.3 of the UGC Act, 1956)

**End Semester Examination – Nov/Dec – 2016**

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|  |  | **Semester :** | **2016-17 ODD** |
| **Code :** | **16PH2004** | **Duration :** | **3hrs** |
| **Sub. Name :** | **Semiconductor Logic Devices** | **Max. marks :** | **100** |

**ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)**

|  |  |  |  |  |
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| **Q. No.** | **Sub Div.** | **Questions** | **Course**  **Outcome** | **Marks** |
| 1. | a. | Convert Binary (11111001001) to decimal | CO1 | **4** |
| b. | Convert decimal (292) to binary | CO1 | **4** |
| c. | Binary addition: 1100.011 + 1011.011 | CO1 | **4** |
| d. | Binary subtraction :11.01111-10.01001 | CO1 | **4** |
| e. | Convert hexa (7 C 9) to decimal | CO1 | **4** |
| **(OR)** | | | | |
| 2. |  | Draw the symbol, timing diagram and truth table for the following gates:  AND, OR, NOT, Ex-OR,NOR and NAND | CO3 | **20** |
| 3. | a. | Obtain the Boolean expression using K-Map  f (A,B,C,D)= Σ (0,1,2,5,7,8,9,10,13,15) | CO3 | **14** |
|  | b. | Obtain the Boolean expression using K-Map  f(A,B,C) =∏ (1,3,5,7) | CO3 | **6** |
| **(OR)** | | | | |
| 4. | a. | Draw the circuit diagram, truth table and derive the K-map for half and full adder. | CO3 | **16** |
|  | b. | Write the Boolean expression for the following circuit  C:\Users\admin\Desktop\2.png | CO3 | **4** |
| 5. |  | Simplify the following Boolean function by using Quine-Mcluskey Method  F(A,B,C,D) =Σm (0,2,3,6,7,8,10,12,13) | CO1 | **20** |
| **(OR)** | | | | |
| 6. | a. | Design a digital comparator with neat truth table and circuit diagram. | CO2 | **18** |
|  | b. | Expansion of SOP and POS. | CO1 | **2** |
| 7. | a. | Derive the expression for 1:4 Demultiplexer and draw the circuit diagram. | CO2 | **10** |
|  | b. | Implement the following Boolean function using 8:1 Mux (7)  F(P,Q,R,S)=Σm (0,1,3,4,8,9,15) | CO2 | **10** |
| **(OR)** | | | | |
| 8. | a. | Implement the following multiple output combinational logic circuit using 4:16 line decoder IC and external gates  F1=Σm (2,3,9,11) F2= Σm (10,12,13,14) F3= Σm (2,4,8) | CO2 | **10** |
|  | b. | Tabulate Decimal number to BCD encoder. | CO2 | **10** |
|  | | **Compulsory:** |  |  |
| 9. | a. | Difference between latches and Flip flops. | CO2 | **4** |
|  | b. | Discuss in detail the different types of flip flops with a neat diagram and truth table. | CO2 | **16** |